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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/037,861	01/02/2002	Yan Chong	015114-054810US	4806

26059 7590 04/12/2006

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EXAMINER	
TRAN, VINCENT HUY	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 04/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/037,861	CHONG ET AL.	
	Examiner	Art Unit	
	Vincent T. Tran	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-15,17-24, 27-56* is/are rejected.

7)☒ Claim(s) *16, 25-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *1/02/02* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to amendment filed on 02/06/2006. Claims 14-56 are pending for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 48 recites the limitation "filed programmable gate array" in line 2. There is insufficient antecedent basis for this limitation in the claim. Lack support in the specification.

4. Claim 53 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: "a second input buffer" it is unclear if there is a first input buffer.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 14 is rejected under 35 U.S.C. 102(b) as being anticipated by Funaba et al. (Funaba) U.S. Patent 6,212,127.

7. As per claim 14, Funaba discloses an integrated circuit comprising:

a series of circuits [103, 108 fig. 1; 202 fig. 21];

a phase detector [203 fig. 21] having an first input [212 fig. 21] coupled to an input of the series of circuits [211 fig. 21] and a second input [213 fig. 21] coupled to an output of the series of circuits;

an up/down counter [204 fig. 21; col. 23 lines 4-11] having an input [214 fig. 21] coupled to an output of the phase detector; and

a first variable-delay block [210 fig. 21] having a control input [210 fig. 21] coupled to an output of the up/down counter,

wherein the series of circuits comprises:

a second variable-delay block [202 fig. 21; 103 fig. 1] having a control input [210 fig. 21; 113 fig. 1] coupled to the output of the up/down counter; and

a frequency divider [108 fig. 1].

8. Claims 34-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Vogt et al. (Vogt) U.S. Patent 6,316,980.

As per claim 34, Vogt discloses an integrated circuit comprising:

a first input buffer having an input [DQ fig. 2] coupled to a first pad [inherent];

a double data rate register comprising [230 fig. 2; col. 2 lines 57-61]

register [235 fig. 2] having a data input responsive to a signal at an output of the first input and clock input [DQS fig. 2]; and

a delay circuit [214, 250 fig. 2] comprising:

a up/down counter [254 fig. 2; col. 4 lines 1-12];

and a variable delay block [214 fig. 2] coupled to provide a delay between a signal at the data input of the register and a signal triggered clock input of the register [claim 1].

In summary, Vogt teaches an integrated circuit to calibrate the delay elements to provide proper delay for clocking data into a register in a DDR SDRAM memory devices which uses a double data rate architecture to achieve high speed operation wherein the architect is designed to transfer two data words per clock cycle [col. 1 lines 51-53; col. 2 lines 57-66].

Vogt does not teach expressly a first register having a data input responsive to a signal at an output of the first input buffer and a rising-edge triggered clock input; and

a second register having a data input coupled to the data input of the first register and a falling-edge triggered clock input coupled to the rising-edge triggered clock input coupled to the rising-edge triggered clock input of the first register. However, this feature is deemed to inherent to the Vogt system as lines 57-64 of column 2 show that the double rate architecture is designed to transfer two data words per clock cycle in order to achieve high-speed operation. Therefore, the DDR SDRAM required in pertinent part a rising edge latching register and a falling edge latching register where both is coupled to the DQS line and DQ line.

9. As per claim 35, Vogt discloses a count provided by the up/down counter [254 fig. 2] inherently sets the delay between the signal at the data input of the first register and the signal at the rising edge triggered clock input of the first register.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

12. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

13. Claims 14-15, 19, 21-24, 27-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagawa US 20010046163 in view of Kobayashi et al. (Kobayashi) U.S. Patent 6,509,776

14. As per claim 14, Yanagawa teaches an integrated circuit comprising:

a series of circuits [51-1...4 fig. 3];

a phase detector [53 fig. 3] having an first input [CLK fig. 3] coupled to an input of the series of circuits and a second input [DCLK fig. 3] coupled to an output of the series of circuits;

an up/down counter [52 fig. 3; paragraph 0058; 0066-0072] having an input coupled to an output of the phase detector; and

a first variable-delay block [51-5] having a control input coupled to an output of the up/down counter,

wherein the series of circuits comprises:

a second variable-delay block [51-4] having a control input coupled to the output of the up/down counter.

However, Yanagawa does not teach the series of circuits comprises a frequency divider.

Kobayashi teaches another integrated circuit relates to a DLL circuit operable to control the phase of the external clock signal and the phase of the internal clock signal in order to guarantee a correct high-speed operation of a synchronous DRAM which controlled by an internal clock signal generated based on an external clock signal; wherein the circuit comprising

a series of circuits [1, 5, 11, 9 fig. 10];

a phase detector [8 fig. 10] having an first input [S2 fig. 10] coupled to an input of the series of circuits and a second input [N5 fig. 10] coupled to an output of the series of circuits.

a delay control circuit [12 fig. 10] having an input [13 fig. 10] coupled to an output the phase detector. Specifically, Kobayashi teaches the series of circuit comprises:

a variable delay block [1-1 fig. 10] having a control input coupled to the output of the delay control circuit; and

a frequency divider.

Yanagawa and Kobayashi are analogous art because they from the same similar problem solving area – to ensure proper data transfer at high-speed.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have modified the series circuit of Yanagawa with the inclusion of a frequency divider of Kobayashi.

The suggestion/motivation for doing so would have been to reduce power consumption as taught by Kobayashi [col. 3 lines 1-13; col. 7 lines 18-22; col. 11 lines 39-43].

Therefore, it would have been obvious to combine Yanagawa with Kobayashi to obtain the invention as specified in claim 1.

15. As per claim 15, Yanagawa teaches an integrated circuit relates to a controller for a semiconductor memory device that outputs data of a double data rate together with a strobe signal, and relates to a system that control data of a double rate by a strobe signal [paragraph 0004]. Specifically, Yanagawa teaches the memory device is configure to operate at a double data rate, and performs the outputting and inputting of data at rising edges and falling edges of a strobe signal [paragraph 0047]. Therefore, the integrated circuits is inherently comprising a first register having an input coupled to an output of the input buffer and a clock input coupled to an output of the first variable-delay block; and

a second register having an input coupled to the output of the input buffer and a complementary clock input coupled to the output of the first variable-delay block. The Yanagawa system would not able to operate at a double data rate if the integrated circuit does included the above registers.

16. As per claim 19, it is noted that the limitations do not differ from claim 1. As demonstrated previously, the combination of Yanagawa and Kobayashi anticipated the limitations in claim 1, therefore claim 19 is rejected for the same reason.

17. As per claim 21, Kobayashi teaches the first variable delay block [1-1 fig. 10] is configured to receive the first clock signal [S2 fig. 10] and the first frequency divider is configured to receive an output from the first frequency divider.

18. As per claim 22, see discussion in claim 15.

19. As per claim 23, inherent [see fig. 1 of Yanagawa].

20. As per claim 24, Yanagawa teaches an synchronous dynamic random access memory configured to receive an output of the first flip-flop and an output of the second flip-flop [paragraph 0047].

21. As per claim 27, Yanagawa teaches the integrated circuit is a programmable logic device [fig. 1].

22. As per claim 28, Yanagawa teaches a computer comprising:

a multiple-data-rate memory [11 fig. 1]; and

the integrated circuit of claim 14 [10 fig. 1] coupled to the multiple-data-rate-memory.

23. As per claim 29, Yanagawa teaches the multiple-data-rate memory is a double-data-rate memory [11 fig. 1].

24. As per claim 30, Yanagawa teaches an integrated circuit comprising:

a series of circuits comprising [51-1...4 fig. 3] comprising:

a first delaying mean [51 fig. 3] for delaying a clock signal by a first duration, wherein the series of circuits receives a first clock signal [CLK fig. 3] and provides a second clock signal [DCLK fig. 3], the second clock signal delayed from the first clock signal;

phase detector means [53 fig. 3] for receiving the first and second clock signals, and providing an output;

a second delaying means [51-5 fig. 3] for delaying a third clock signal [DS fig. 3] by a second duration; and

adjustment means [52 fig. 3] for increasing or decreasing the first and second durations based on the output of the phase detector means [paragraph 0058-0062].

However, Yanagawa does not teach a series of circuits comprising a dividing means for dividing a frequency of the first clock signal.

Kobayashi teaches a series of circuit comprising:

a dividing means [6 fig. 10] for dividing a frequency of a clock signal; and a delaying means [1-1] for delaying a clock signal by a duration, wherein the series of circuits receives a first clock signal [S2 fig. 10] and provides a second clock signal [N5 fig. 10], the second clock signal delayed and divided in frequency from the first clock signal [see further discussion in claim 1];

Therefore, it would have been obvious to combine Yanagawa with Kobayashi to obtain the invention as specified in claim 30.

25. As per claim 31, Kobayashi teaches the series of circuit [1 fig. 10] provides the second clock signal [N5 fig. 10] by first dividing the frequency of the first clock signal.

26. As per claim 32, Kobayashi teaches the frequency of the first clock signal is divided by a value selected from the group consisting of 4, 8, and 16 [col. 10 lines 62-64].

27. As per claim 33, Kobayashi teaches the series of circuits provides the second clock signal by delaying the first clock signal before dividing its frequency [fig. 10].

28. Claims 17-18, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagawa and Kobayashi as applied to claim 14 or 19 above, and further in view of Fiscus U.S. Patent 6,492,852.

29. As per claim 17, Kobayashi teaches the frequency divider having an input coupled to the output of the variable-delay block and not an input of the variable-delay block coupled to an output of the frequency divider. Such that, there existed a problem in the design since only the control circuit is operated at a reduced rate/power, leaving the delay chain operating at the original higher rate/power levels.

Fiscus teaches another integrated devices and more particularly, to an improved delay locked loop circuit design for power conservation that synchronizes a system clock with data

line. Specifically, Fiscus teaches an input of the variable delay block [105 fig. 5] is coupled to the output of the frequency divider.

At the time of the invention was made, it would have been obvious to one ordinary skill in the art to have modified the integrated circuit of Yanagawa/Kobayashi with the frequency divider of Fiscus in order to conserve power on the variable delay line [col. 2 lines 46-52; col. 4 lines 15-25].

30. As per claim 18, Fiscus teaches the output of the frequency divider is coupled to an input of the variable delay block.

31. As per claim 20, Fiscus teaches the first frequency divider is configured to receive the first clock signal and the first frequency divider is configured to receive an output from the first variable delay block [fig. 5].

32. Claims 34-50, 53 is rejected under 35 U.S.C. 103(a) as being unpatentable over McCracken et al. (McCracken) U.S. Patent 6,279,073 in view of Murakami US 20010004335 and Vogt.

33. As per claim 34, 42, 50, McCracken teaches an integrated circuit comprising:

a data signal couple to a first pad [150 fig. 4, fig. 1];

a first register [174 fig. 4] having a data input [172 fig. 4] responsive to a data signal and a rising-edge triggered clock input [152 fig. 4 – strobe signal];

a second register [176 fig. 4] having a data input coupled to the data input of the first register and a falling-edge triggered clock input [178 fig. 4] coupled to the rising-edge triggered clock input of the first register; and

a delay circuit [102 fig. 2] comprising:

a control circuit [not show – to control the strobe delay 112 fig. 3];

a series of delay circuit [122s fig. 3]coupled to provide a delay between a signal at the data input of the first register and a signal at the rising-edge triggered clock input of the first register; and

a multiplexer [108 fig. 3] having a first input [strobe signal fig. 3] coupled to an input of the delay circuit [122 fig. 3 and a second input coupled to an output of the delay circuit [fig. 3].

However, McCracken does not explicitly teach a first input buffer having an input coupled to a first pad nor a control circuit having an up/down counter;

Murakami teaches another system related to a synchronous double data rage and more particularly to an improvement of the read/write performance of a DDR SDRM. Specifically, Murakami teaches a integrated circuit comprising:

a data signal coupled to a first pad [DQ fig. 3]; and

a data register having a data input responsive to a signal at an output of the first input buffer and a rising-edge triggered clock input [fig. 4].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art the have modified the circuit of McCracken with an input buffer to buffer the data signal as teach by Murakami since the method of buffer the input data is such an old and well know art in the field of computer.

And Vogt teaches another integrated circuit related the calibrating of the delay elements to provide proper delay for clocking data into a register in a DDR SDRAM memory devices which uses a double data rate architecture to achieve high speed operation wherein the architect is designed to transfer two data words per clock cycle. Specifically, Vogt teaches a control circuit [250 fig. 2] including an up/down counter [254 fig. 2].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the control circuit of McCracken with the up/down counter of Vogt to dynamically increments or decrements a count depending on whether the reference signal leads of lags in order to provide proper delay for clocking data into the register since the up/down counter is well know in the art for delay control.

34. As per claim 35, Vogt discloses a count provided by the up/down counter [254 fig. 2] inherently sets the delay between the signal at the data input of the first register and the signal at the rising edge triggered clock input of the first register.

35. As per claim 36, McCracken teaches a bypass path [118 fig. 3] to bypass the variable delay element.

36. As per claim 37, McCracken teaches a multiplexer [108 fig. 3] having a first input [strobe signal 118 fig. 3] coupled to an input of the variable delay element and an output coupled to an output of the variable delay element [42 fig. 3].

37. As per claim 38, the combine teachings of McCracken and Murakami teaches a second input buffer [Strobe buffer fig. 1 of Murakami] coupled to a second pad to receive a DQS signal,

wherein the rising edge triggered clock input of the first register [174 fig. 4 of McCracken] is responsive to a signal at the output of the second input buffer [Strobe signal in McCracken], and a DQ signal [150 fig. 4 of McCracken or DQ fig. 1 of Murakami] is received at the first pad.

38. As per claim 39, Vogt teaches a clock signal is used in generating the count provided by the up/down counter [250 fig. 2 reference clock signal].

39. As per claim 40, McCracken teaches a plurality of programmable logic elements [12 fig. 1], configurable to perform user-defined logic functions; and

a plurality of logic interconnect lines [28-32 fig. 1] configurable to couple the plurality of programmable logic elements to the double-data race register [44 fig. 1].

40. As per claim 41, McCracken teaches the variable delay block comprises a series of delay element [122s fig. 3].

41. As per claim 43, see discussion in claim 35.

42. As per claim 44, see discussion in claim 36.

43. As per claim 45, see discussion in claim 38.

44. As per claim 46, see discussion in claim 39.

45. As per claim 47, see discussion in claim 40.

46. As per claim 48, McCracken teaches a technique for allowing various DDR SDRAM configuration to be used with the configurable synchronizer. Therefore, it is obvious to one of ordinary skill in the art that McCracken also teach the integrated circuit is a filed programmable gate array.

47. As per claim 49, see discussion in claim 41.

48. As per claim 53, see discussion in claim 38.

49. Claims 50-52, 54-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCracken in view of Vogt.

50. As per claim 50, McCracken teaches an integrated circuit comprising:

a rising-edge triggered register [174 fig. 4] having a data input [170 fig. 4] and a clock input [152 fig. 4];

a falling edge triggered register [176 fig. 4] having a data input coupled to the data input of rising-edge triggered register and a clock input coupled to the clock input of the rising edge triggered register;

a series of delay [122 s fig. 3] coupled to provide a variable delay between a signal at the data input and a signal at the clock input of the first register ;

a multiplexer [108 fig. 3] having an input coupled to an input of the series of delay circuits and an output coupled to an output of the series of delay circuits; and

Vogt teaches a counter [254 fig. 2] having an output coupled to series of delay circuits [214 fig. 4 - see discussion in claim 42].

51. As per claim 51, Vogt teaches the counter provides a count to the series of delay circuits; wherein the count is incremented and decremented to vary the variable delay [col. 4 lines 7-12];

52. As per claim 52, McCracken teaches the multiplexer [108 fig. 3] provides a bypass path for bypassing the series of delay circuits.

53. As per claim 54, see discussion in claim 39.

54. As per claim 55, see discussion in claim 40.

55. As per claim 56, McCracken teaches an output of the rising edge triggered register is coupled to a memory. Therefore, it is obvious to one of ordinary skill in the art that the memory of McCracken included the claimed FIFO memory because the special structure of the claimed memory does not alter the operation of the integrated circuit.

Allowable Subject Matter

56. Claims 16, 25, 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Tran